REMARKS/ARGUMENTS

Claims 1-17 are pending in the application.

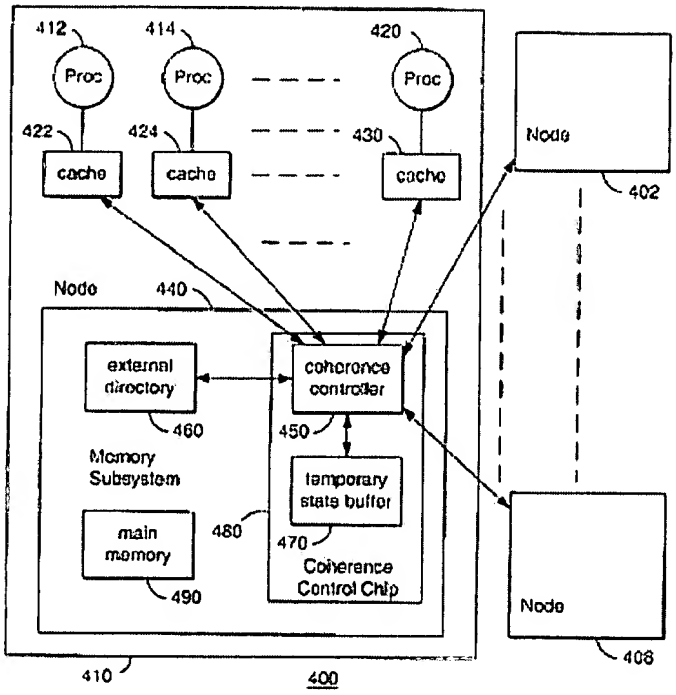
Claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,560,681 to Wilson, or US Patent 6,668,308 to Barroso. Claims 5, 13, and 15-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wilson in view of Jim Handy, "The Cache Memory Handbook". Applicants respectfully disagree, since neither Wilson nor Barroso teaches the cache-coherent input/output device recited in claims of the present application.

I. Rejections under 35 U.S.C. §102(e)

A. Wilson

Claim 1 is directed to a cache-coherent input/output device comprising a plurality of sub-unit caches, each assigned to one of a plurality of port components; and a coherency engine coupled to the plurality of sub-unit caches.

The Examiner has asserted that Fig. 4 of Wilson discloses a cache-coherent I/O device. Applicants respectfully disagree, since what is shown in Fig. 4 of Wilson is a block diagram of a ccNUMA system having a number of interconnected nodes each including a number of processors and caches (Wilson, col. 5, lines 1-3). Fig. 4 of Wilson does not show a cache-coherent I/O device.



The Examiner has asserted that elements 412 and 414 in Fig. 4 of Wilson teach the recited port components. Applicants respectfully disagree, since these elements are processors. Wilson states:

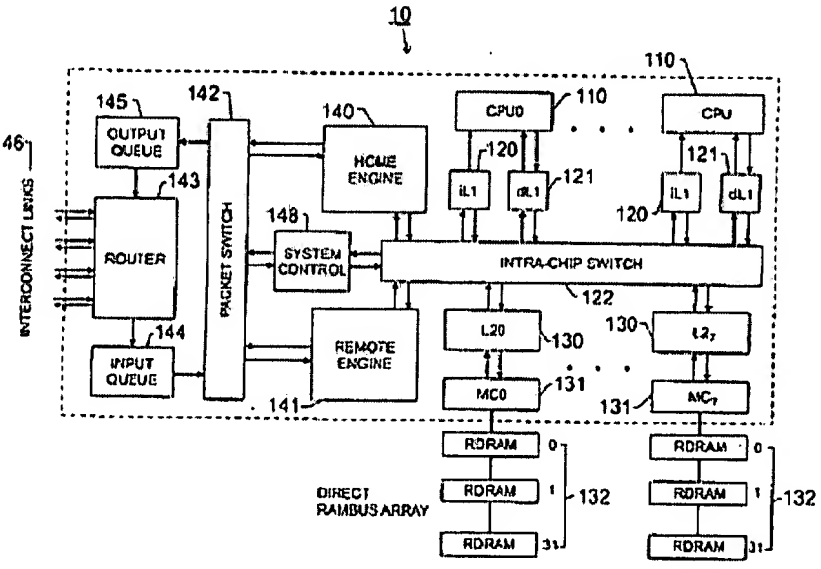
> FIG. 4 shows an overview of a ccNUMA system 400 comprising a number of connected nodes 402, . . . , 408, and 410. Each node, as shown for node 410, includes some number of processors 412, 414, . . . , and 420 having respective caches 422, 424, . . . , and 430 connected to a single memory subsystem 440 (Wilson, col. 5, lines 26-31, emphasis added).

However, "port components" are defined in the present application as "any suitable component for CPU ports (Specification, the sentence bridging pages 3 and 4). Processors do not fall into the scope of port components.

Thus, Wilson fails to teach the cache-coherent input/output device recited in independent claims 1, 6 and 9, and fails to teach the port components recited in independent claims 1 and 6. Accordingly, Applicants respectfully submit that claims 1-17 are patentable over Wilson.

B. Barroso

The Examiner has asserted that Fig. 1 of Barroso teaches a cache-coherent I/O device. Applicants respectfully disagree, since Fig. 1 of Barroso shows a block diagram of a single PIRANHA processing chip, which is a chip-multiprocessing system, not a cache-coherent I/O device (Barroso, col. 3, lines 21-23; and Abstract).



BLOCK DIAGRAM OF A SINGLE-CHIP PIRANHA PROCESSING NODE

FIG. 1

The Examiner has asserted that elements 110 in Fig. 1 of Barroso teach the port components recited in the claims. Barroso states:

> FIG. 1 shows the block diagram of a single PIRANHA™ processing chip 10. Each ALPHA™ CPU core (central processing unit or CPU) 110 is directly connected to dedicated instruction (iL1) and data cache (dLI) modules 120 and 121 (Barroso, col. 6, lines 43-47, emphasis added).

But again, such elements are central processing units, not port components.

Thus, Barroso fails to teach the cache-coherent input/output device recited in independent claims 1, 6 and 9, and fails to teach the port components recited in independent claims 1 and 6. Accordingly, Applicants respectfully submit that claims 1-17 are patentable over Barroso.

II. Rejections under 35 U.S.C. 103(a)

Claims 5, 13 and 15-17 recite a cache-coherent input/output device, and claim 5 further recites port components. As discussed above, Wilson fails to teach the cache-coherent input/output device or the port component. Handy discloses a protocol for use in a multiple processor system with multiple caches, and does not supply any deficiency of Wilson.

Accordingly, Applicants respectfully submit that claims 5, 13 and 15-17 are patentable over the combination of Wilson and Handy for these additional reasons.

Conclusion

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600**.

Respectfully submitted,

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